Remarks:

<u>Claim Rejections – 35 USC 112</u>

Claim 2 was rejected under the second paragraph of 35 USC 112 as being indefinite because n+ region and p+ region are recited twice. However, the first recitation refers to the structures formed in the n-well and the second recitation refers to the structures formed in the p-well, thus there is no ambiguity insofar as the regions are clearly defined with respect to their location. However, in order to simplify the reading of the claim applicant has added the terminology proposed by the examiner.

Also, since the n+ region in the p-n junction and the p+ region in the p-n junction both refer to the p-n junction, both are clearly defined since the p-n junction is defined in the claims. Again therefore there is no ambiguity. However, to avoid further argument on this point, applicant has amended the claim 2 to specifically refer to these regions as the "additional" p+ and n+ regions.

The Office action states that the p-n junction is formed between two materials. It is correct that a diode is made up of a p and an n material (anode and cathode). In this case the n-material is defined by an <u>additional</u> n+ region and two p-doped material of different doping density as defined by the p-well, and a highly doped region defined by the additional p+ region which forms the anode of the diode. Hence, both the low doped p-well and the highly doped additional p+ region are included in the recitation of the diode structure.

<u>Claim Rejections – 35 USC 103</u>

Claims 2-4 were rejected over Ker in view of Yu

Regarding claim 2, the Office Action states that Ker <u>teaches a method of increasing the holding voltage</u> of an LVTSCR structure. This is not correct. Ker seeks to reduce the triggering voltage not increase the holding voltage as was discussed in response to the previous Office action.

In particular Ker makes use of a SOI (silicon over insulator) process to address the holding voltage problem that is otherwise found in SCRs. See Description of the Related Art in

Ker, column 1, lines 21-24. Ker instead is providing a different type of SCR structure in which the triggering voltage is reduced (see Description of the Related Art in Ker, column 1, lines 15-59 discussing the problem that Ker is seeking to address)

The Office action goes on to state that Ker teaches one additional p+ region 222 and one n+ region 220. However, claim 2 was previously amended to refer to at least one additional n+ region. As discussed in response to the previous Office action, 220 is part of the cathode. Claim 2 requires forming an additional n+ region in the p-well while Ker has only the n+ region in the p-well that is typically found in an LVTSCR and which is defined in claim 2 as the second n+ region. Thus Ker differs structurally from the present invention in that it does not have an additional n+ region in the p-well in addition to the second n+ region.

Regarding claims 3-4, the same arguments are made in the Office Action about Ker teaching a method of increasing the holding voltage of an LVTSCR and forming at least one additional p+ region 222 and at least one n+ region 220 inside the p-well. As discussed above, Ker does not teach either of these two aspects.

Regarding claims 3 and 4, the Office Action reiterates the arguments from the previous Office action that Ker does not teach in Figure 8B an n+ region and a p+ region but teaches a diode 324 and that Yu teaches an n+ region and a p+ region in a p-substrate.

As discussed in the previous response, Ker does contemplate the use of an external diode series – see also the discussion at column 11, lines 33-35. It is specifically this inclusion of external diodes that the present invention seeks to avoid as is clear from the discussion in the acknowledged prior art in its Background section at page 7, lines 6-13. The present invention seeks to provide a solution to the inherent problems involved in such an external diode string. This further shows that Ker teaches only external diodes and does not suggest integrated diodes in the LVTSCR structure.

In fact Ker itself discloses in Figure 8A a p-substrate with p+ and n+ regions. In fact, as early as 1998, in patent 5,754,380 the same inventor Ker taught a p-substrate with p+ region and n+ region. However, in spite of being aware of the existence of diodes in a p-substrate, this did not suggest to Ker to create an integrated set of diodes in an LVTSCR structure as proposed by the present invention to address the latch-up problem. As mentioned above, Ker instead addresses latch-up by making use of a SOI process. In the same way, any other person skilled in the art, faced with the problem of latch-up in LVTSCRs and having Ker at his disposal, would

recognize that the SOI process used by Ker already addresses the latch-up problem, thereby not requiring additional diodes to address latch-up.

It is therefore not surprising that there is no teaching or even a suggestion in either of the cited references to include integrated diodes to avoid the latch-up problem of an LVTSCR. Therefore it cannot be said to be obvious to combine the two cited references to achieve the benefits discussed by the present application at page 9, line 23 to page 10, line 12, namely: *"It provides for a simple interconnect layout and a compact design by providing a straightforward serial arrangement. Simulation results have also shown that compared to prior art high holding voltage SCR designs, the present invention displays little sensitivity to process variations, doping levels, and dimension variations. Figure 8 shows voltage curves 800, 802, and 804 for widths w=25μm, 50μm, and 100μm, respectively. Furthermore, since the diodes are formed inside the grounded p-well 402, the structure does not increase the capacitance over that of a conventional LVTSCR. This is illustrated by the curves in Figure 9 showing the capacitance variation with drain-source bias for a conventional device (curve 900) compared to that of a device of the invention (curve 902). Figure 9 also shows that the conductance curves for a device of the invention (curve 904) remains essentially the same as that for a conventional LVTSCR (curve 906). Furthermore, the holding voltage displays a low temperature curve. Referring to Figure 10, the lattice temperature variation for a device of the invention (curve 1000) is substantially the same as that for a conventional device (curve 1002). Also, the holding voltage is shown to be higher for the device of the invention."* (underlining was added for emphasis)

There is nothing in Ker that suggests that Ker is aware of the above benefits. The only issue above that is addressed by Ker is the high holding voltage in order to reduce latch-up, which Ker addresses in an entirely different way, by making use of a SOI process.

The Office action goes on to refer to Yu as teaching a diode formed in a p-substrate. As pointed out in response to the previous Office action, applicant does not deny that diodes formed in a p-substrate exist in the prior art. However, there is nothing in Yu to suggest combining the reference with Ker, and as discussed above, Ker, in spite of being aware of integrated diodes does not teach of suggest this. Thus there is nothing in either of the references to suggest the forming of an integrated diode in the p-well as taught by the present invention.

Response to Arguments

The Office Action states that the recitation of increasing the holding voltage occurs in the preamble and is therefore not given patentable weight . However, we are dealing here with method claims and not product claims, therefore the recitation in the preamble defines the claim and forms part of the claim, and should be given patentable weight.

In any event, the recitation of increasing the holding voltage also goes to obviousness and whether the combining of the two references, Ker and Yu can be said to be taught or suggested by either of the references. Since neither Ker nor Yu suggest addressing <u>holding voltage issues</u> by including diodes in a structure and since there is nothing explicit in Ker to include such additional diode structures or to combine Ker with Yu, it cannot be said to be obvious to combine the two references by including some of the structural details from Yu into the structure of Ker.

On the issue of external and internal diodes, the present invention specifically teaches the inclusion of internal diodes while external diodes are part of the prior art. Thus, insofar as Ker teaches external diodes it teaches only the acknowledged prior art.

Thus Ker differs structurally from claim 2 in that it fails to include at least one <u>additional</u> n+ region in the p-well, and there is nothing to suggest in either of the cited references to add additional n+ regions into the p-well. In fact Ker teaches away from such a suggestion by addressing holding voltage issues using SOI and failing to teach or suggest forming integrated (internal) diodes. In light of the structural differences of the present claims over the cited art, applicant requests that the claims be allowed.

Respectfully Submitted,

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Jurgen K. Vollrath
VOLLRATH & ASSOCIATES
588 Sutter Street #531, San Francisco, CA, 94102
Telephone: (408) 667 1289